a third memory device;

a fourth memory device stacked on the third memory device; and

a second buffer coupled to the third and fourth memory devices and to the first buffer.

18. (Amended once) A memory system comprising:

a bus;

a stack of memory devices;

a buffer coupled between the stack of memory devices and the memory bus;

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the bus.

19. (Amended once) A memory system comprising:

a bus;

a stack of memory devices;

a first buffer coupled between the stack of memory devices and the memory bus;

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the first buffer.

REMARKS

Priority Claim

The specification is amended to claim priority from U.S. Provisional Application Ser. No. 60/232,596 filed September 14, 2000.

Claim Rejections - 35 USC § 102

Claims 1-4, 11-17 and 20-23 are rejected under 35 USC 102(a) as being anticipated by U.S. Patent No. 5,963,716 to Welborn, et al. ("Welborn"). Applicant traverses this rejection.

Claim 1 recites a memory system having a buffer coupled to two memory devices in which the second memory device is stacked on the first memory device. The Examiner alleges that the two memory devices recited in claim 1 read on items DATA A1 and DATA A2 shown in Fig. 4 of Welborn. This rejection, however, is based on an unreasonable interpretation of the terms "memory device" and "stacked". It is clear from claim 1, read in light of the specification, that the term "memory device" as used by Applicants refers to a

physical apparatus, and the term "stacked" refers to the second device being physically stacked on the first.

In contrast, the items DATA A1 and DATA A2 in Fig. 4 of Welborn are nothing more than abstract data constructs. They are data elements (col. 2, line 58) in a data stream (col. 1, line18) that is stored in a buffer (col. 2, line 30). Although the word "stack" appears in the Welborn reference, it is used to describe another abstract data construct in which the physical location of the elements is irrelevant. Again, this is an unreasonable interpretation of the work "stacked" as used by Applicant in claim 1 read in light of the specification.

Although claims terms are given their broadest reasonable interpretation during examination, the interpretation must also be consistent with the interpretation that those skilled in the art would reach. MPEP § 2111. Claim 1 is drawn to a memory system. In contrast, Welborn is drawn to a technology for decompressing data from a data stream. Welborn discloses the use of temporary memory, but this is only tangential to the system. One skilled in the art of memory systems would not interpret Welborn as disclosing a memory system, nor would such a skilled person interpret the terms "memory device" and "stacked" as used in claim 1 as reading on the items DATA A1 and DATA A2 in Fig. 4 of Welborn.

Claim 11 recites that the first and second memory devices are stacked and arranged to capacitively isolate the memory devices from a bus. Capacitive isolation is a physical phenomena. As discussed above, the Welborn reference relates to data abstractions and is irrelevant to the invention recited in claim 1. It is untenable to argue that Welborn discloses capacitive isolation between the devices the Examiner alleges are memory devices (data elements DATA A1 and DATA A2) and a bus.

Claim 17 recites a buffer coupled between a stack of memory devices and a bus. Again, from the perspective of one skilled in the art of memory systems, it is clear from the claim language that the stack of memory devices recited in claim 17 includes physical memory devices that are physically stacked. The Examiner has proposed an unreasonable reading of the claim language. Thus, claim 17 is not anticipated by the abstract data constructions described in Welborn.

Allowable Subject Matter

Claims 5-10, 18 and 19 are indicated as being allowable if rewritten in independent form and to include all of the limitations of the base claim and any intervening claims. (Applicant assumes that, in paragraph 3 of the Detailed Office Action, claim 20 should

actually be claim 18 as listed in the Office Action Summary.) These claims have been rewritten as suggested by the Examiner.

Applicant requests reconsideration in view of the foregoing amendments and remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears than an interview would be helpful in advancing the case.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning at page 1, line 1 has been amended as follows:

"This application claims priority from U.S. Provisional Application Ser. No. 60/232,596 filed September 14, 2000 titled "Memory System Having Buffers For Isolating Stacked Memory Devices."

In the Claims:

5. (Amended once) A memory system [according to claim 1 wherein the buffer is a first buffer and further] comprising:

a first memory device;

a second memory device stacked on the first memory device;

a first buffer coupled to the first and second memory devices;

a third memory device;

a fourth memory device stacked on the third memory device; and

a second buffer coupled to the third and fourth memory devices and to the first buffer.

18. (Amended once) A memory system [according to claim 17 further] comprising:

a bus;

a stack of memory devices;

a buffer coupled between the stack of memory devices and the memory bus;

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the bus.

19. (Amended once) A memory system [according to claim 17 wherein the buffer is a first buffer and further] comprising:

a bus;

a stack of memory devices;

a first buffer coupled between the stack of memory devices and the memory bus;

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the first buffer.

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